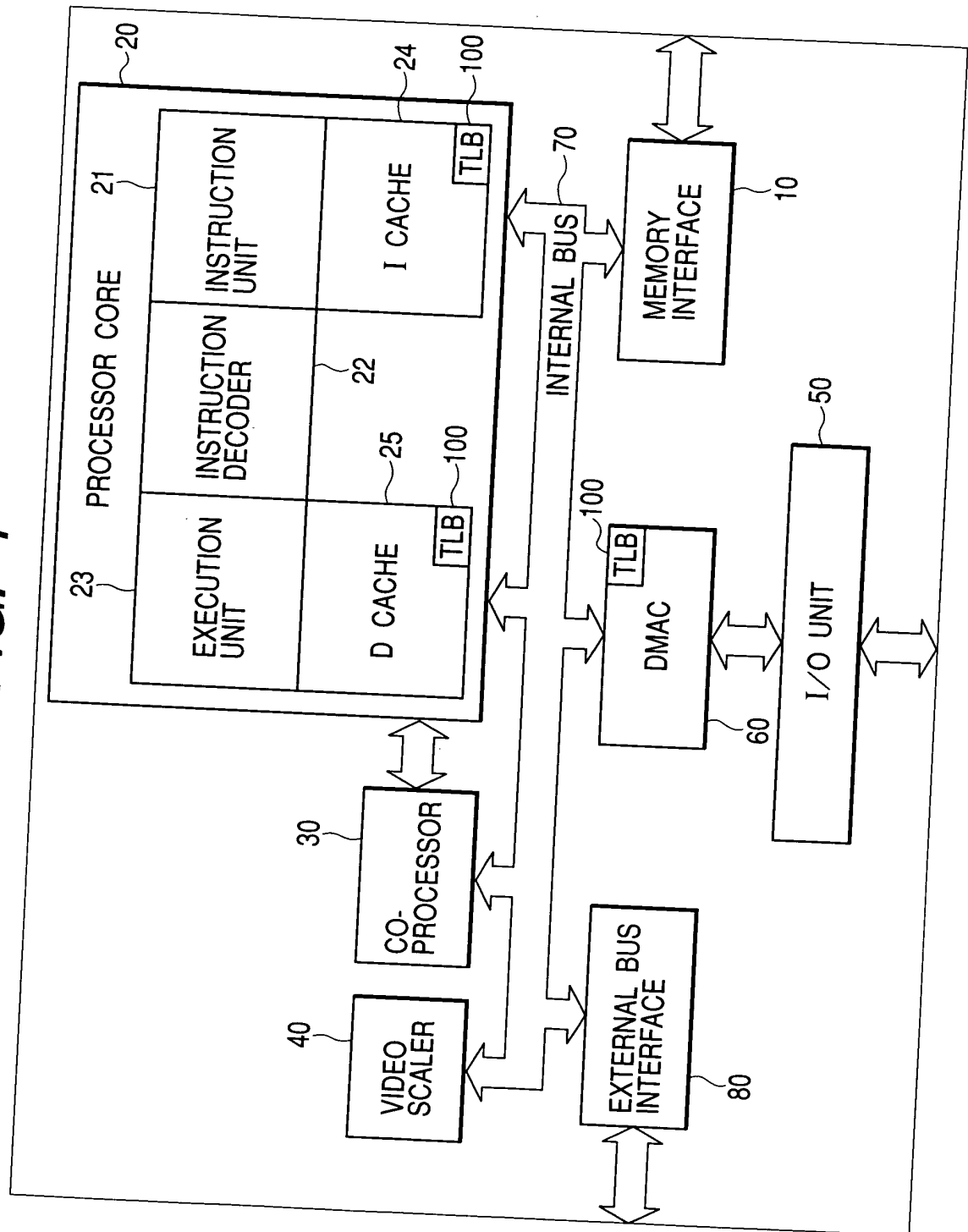


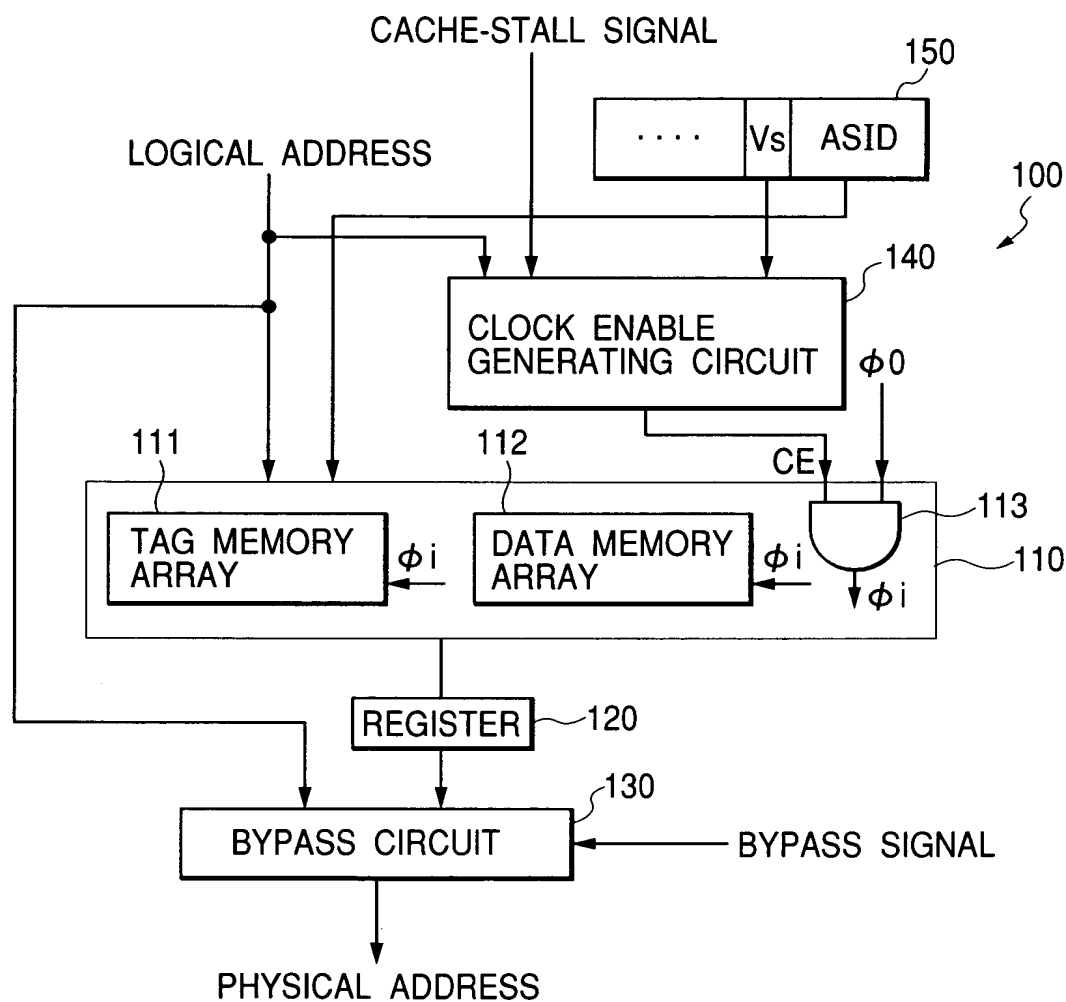
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FIG. 1

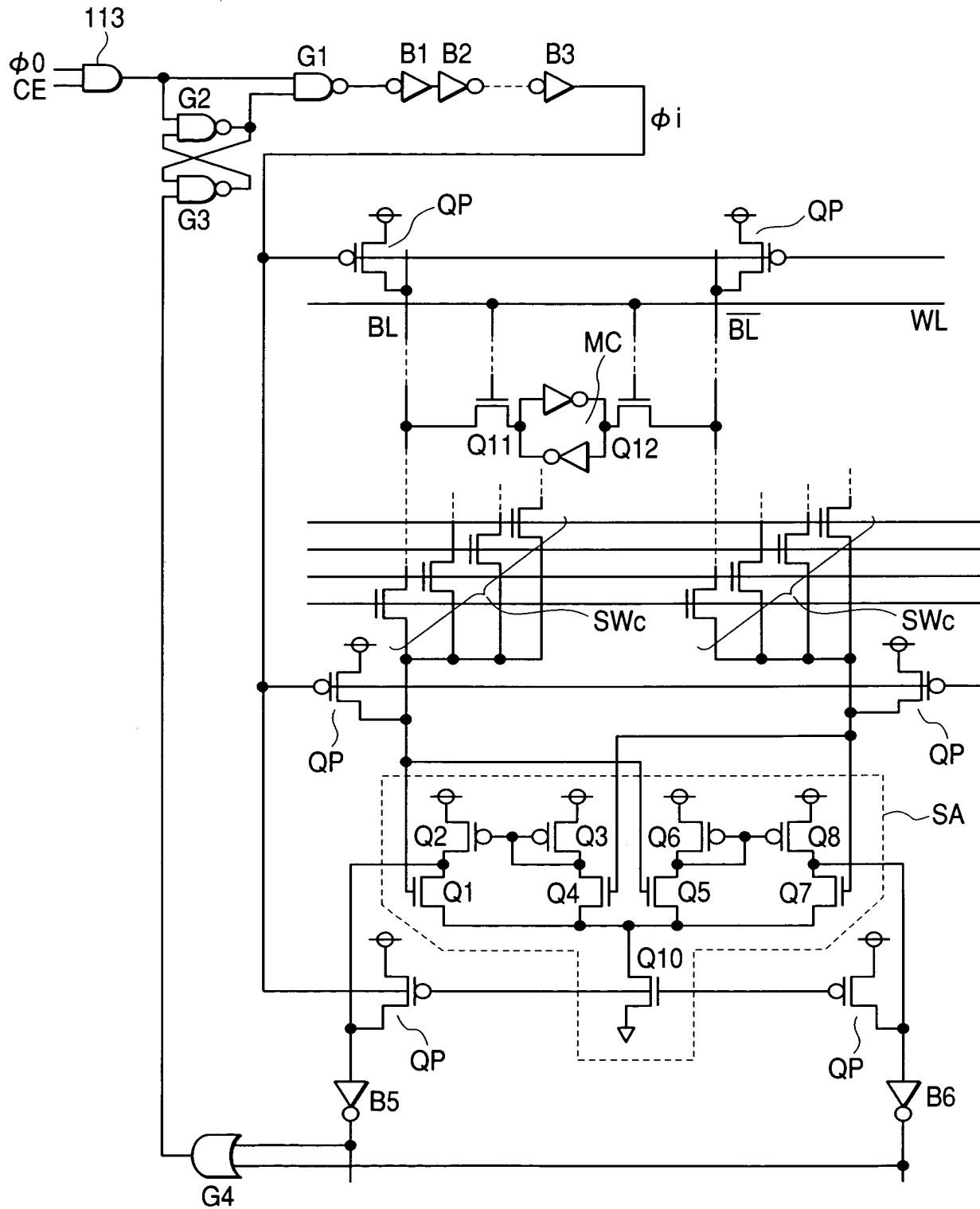


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**FIG. 2**

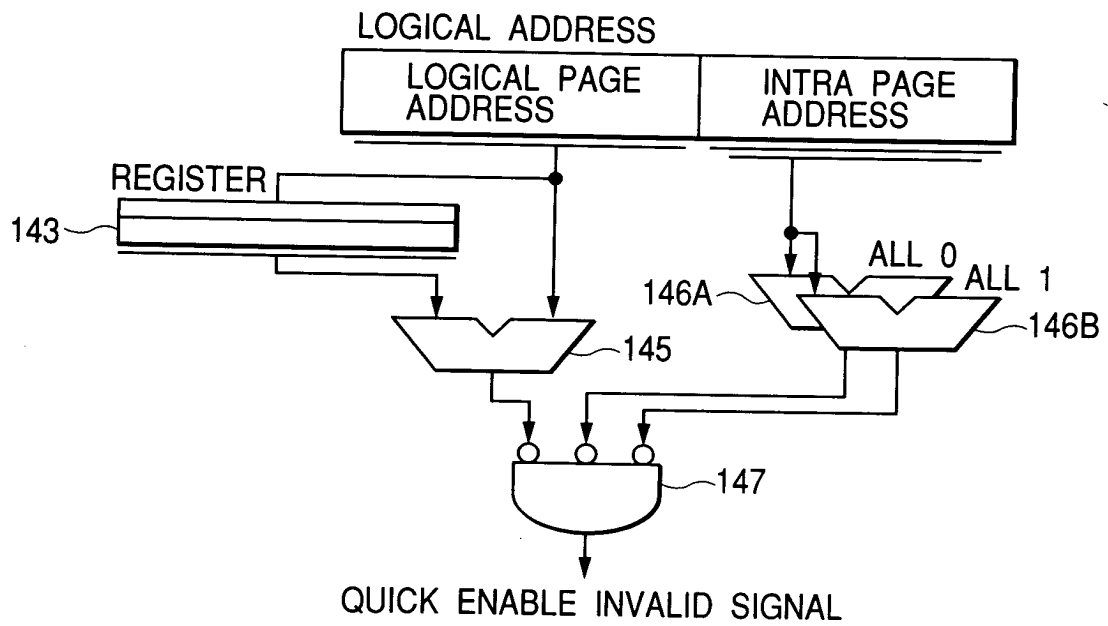


**FIG. 3**



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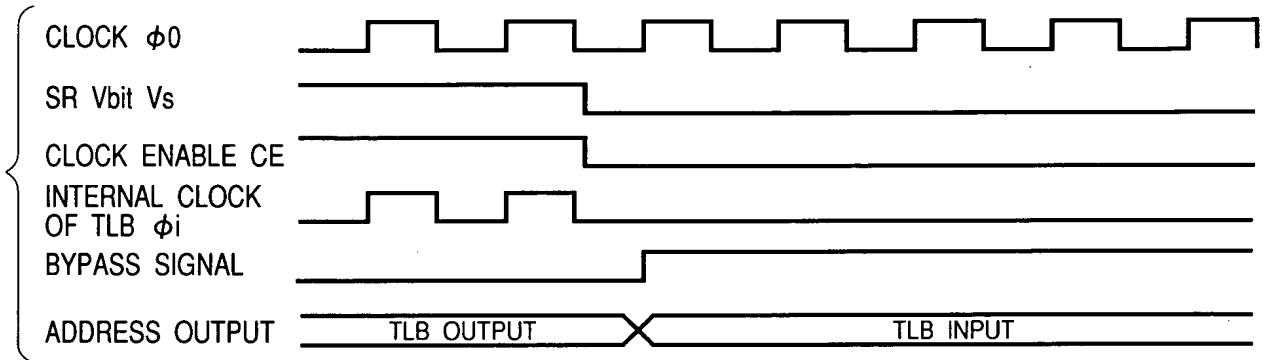
**FIG. 4**



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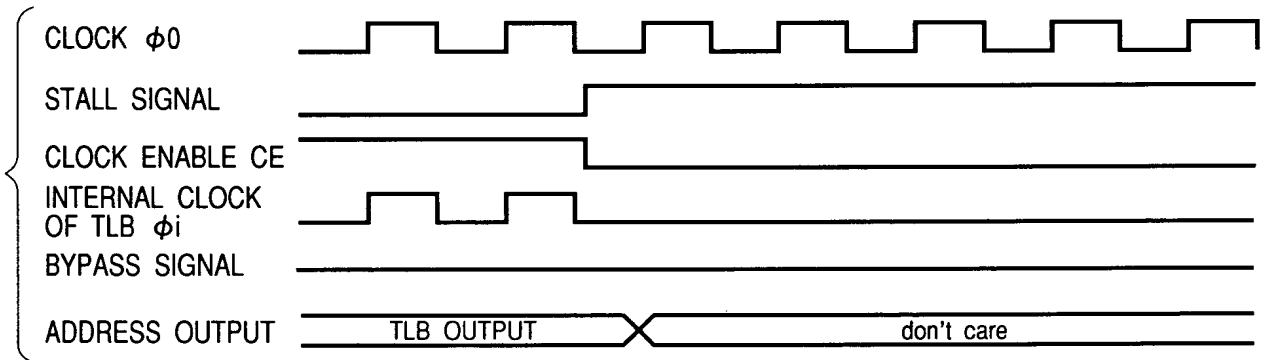
## FIG. 5(a)

V-BIT IS 0 IN THE STATUS REGISTER



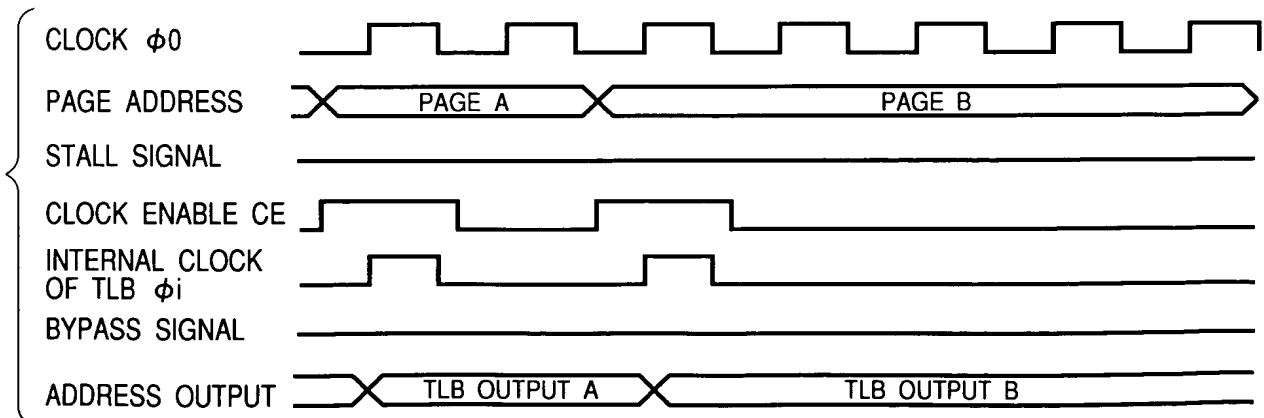
## FIG. 5(b)

CACHE-STALL SIGNAL IS HIGH LEVEL



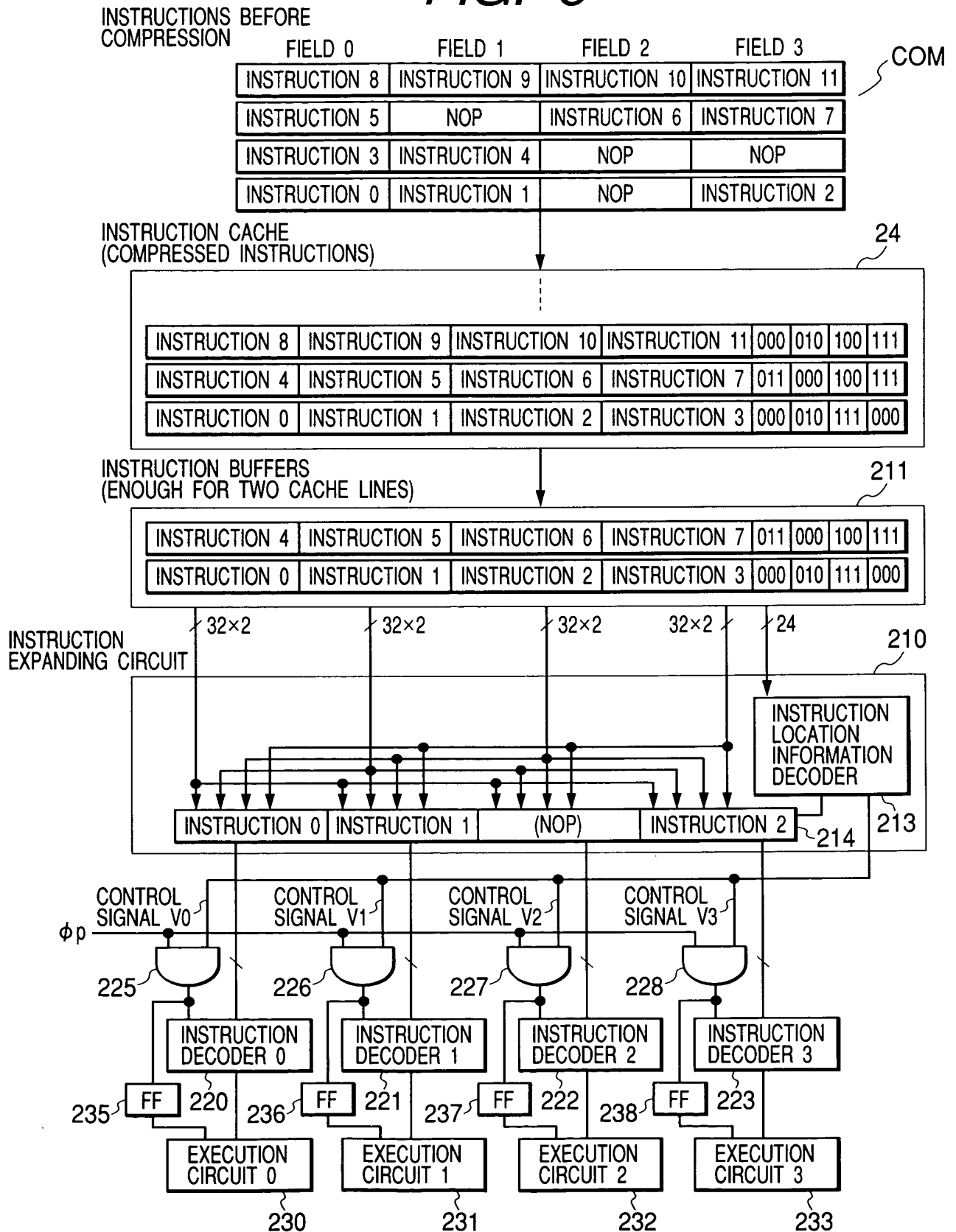
## FIG. 5(c)

SAME PAGE ADDRESS IS ACCESSED



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**FIG. 6**



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FIG. 7

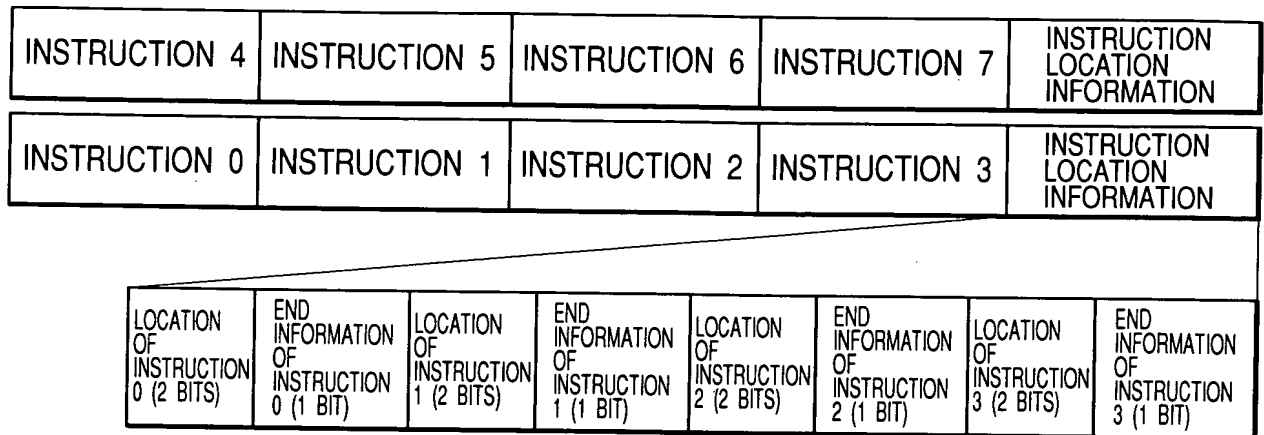


FIG. 8

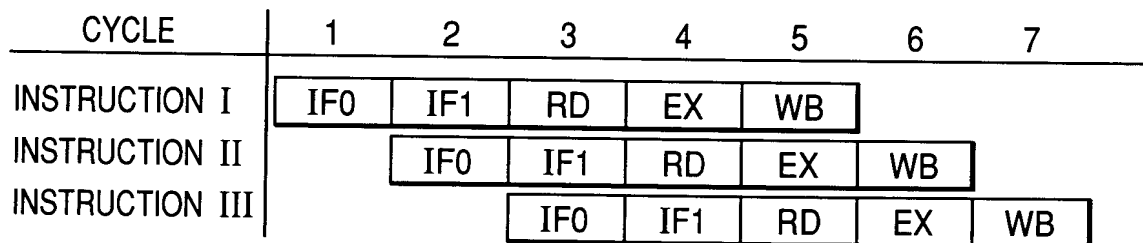
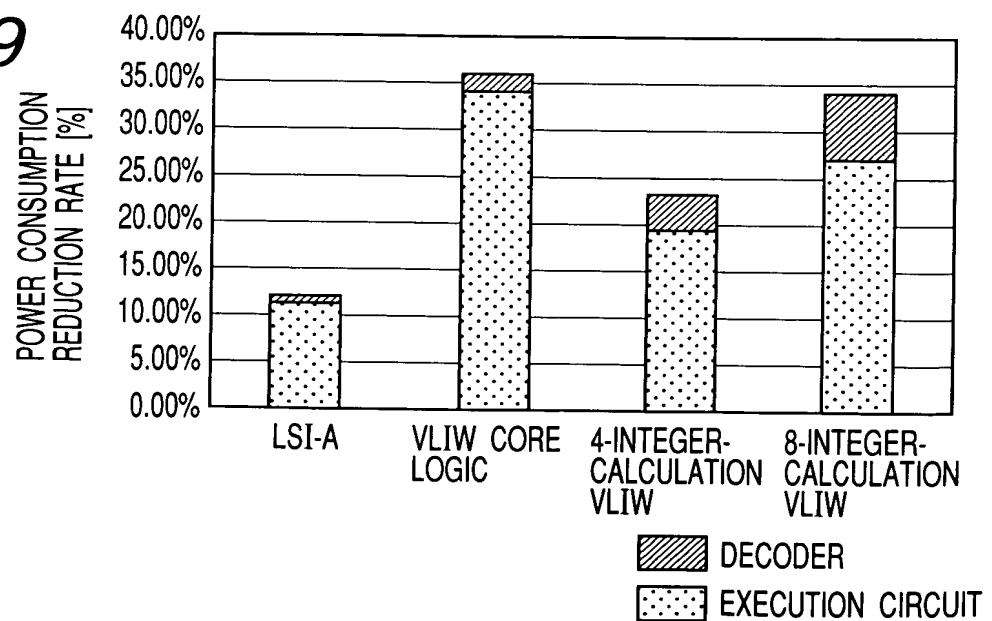
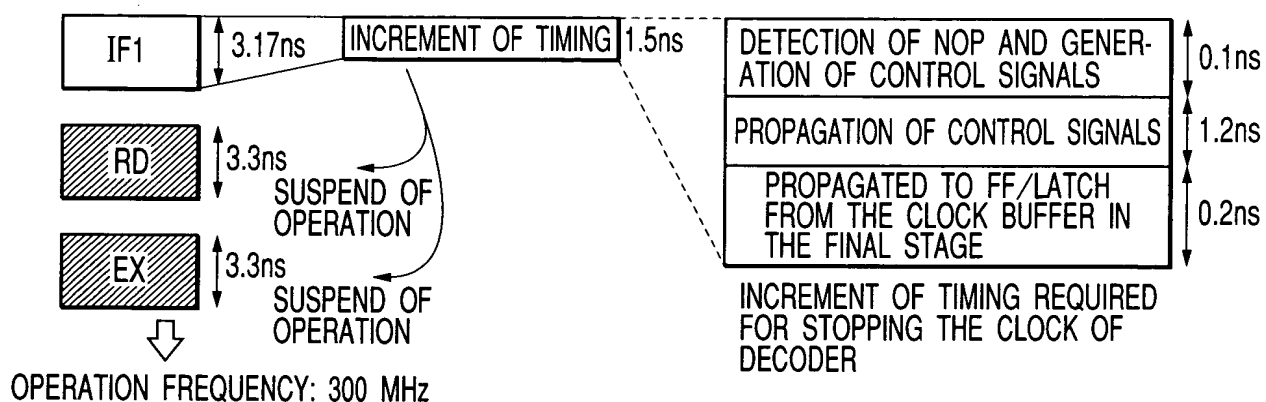


FIG. 9



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*FIG. 10(a)**FIG. 10(b)*